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(54) **MOSFET HAVING DUAL-GATE CELLS WITH AN INTEGRATED CHANNEL DIODE**

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(51) **Int. Cl.**

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H01L 29/40	(2006.01)
H01L 29/10	(2006.01)
H01L 29/861	(2006.01)
H01L 23/50	(2006.01)
H01L 27/06	(2006.01)
H01L 29/423	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 29/7803*** (2013.01); ***H01L 23/50*** (2013.01); ***H01L 27/0629*** (2013.01); ***H01L 29/1095*** (2013.01); ***H01L 29/404*** (2013.01); ***H01L 29/407*** (2013.01); ***H01L 29/4236*** (2013.01); ***H01L 29/42356*** (2013.01); ***H01L 29/7811*** (2013.01); ***H01L 29/7813*** (2013.01); ***H01L 29/861*** (2013.01)

(58) **Field of Classification Search**

CPC H01L 27/10823; H01L 29/407; H01L 29/66704; H01L 27/10876; H01L 27/0629; H01L 29/7803; H01L 29/7811; H01L 29/861

See application file for complete search history.

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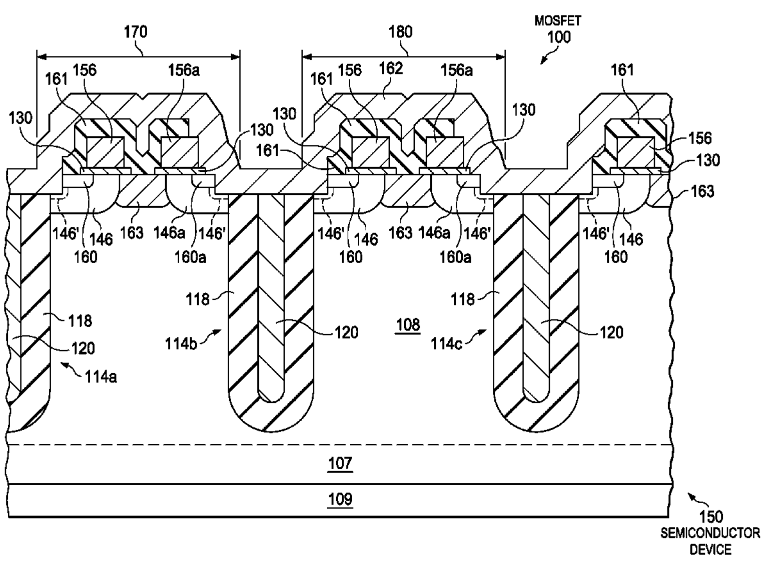
(57) **ABSTRACT**

A semiconductor device includes MOSFET cells having a drift region of a first conductivity type. A first and second active area trench are in the drift region. A split gate uses the active trenches as field plates or includes planar gates between the active trenches including a MOS gate electrode (MOS gate) and a diode gate electrode (diode gate). A body region of the second conductivity type in the drift region abutts the active trenches. A source of the first conductivity type in the body region includes a first source portion proximate to the MOS gate and a second source portion proximate to the diode gate. A vertical drift region uses the drift region below the body region to provide a drain. A connector shorts the diode gate to the second source portion to provide an integrated channel diode. The MOS gate is electrically isolated from the first source portion.

11 Claims, 9 Drawing Sheets



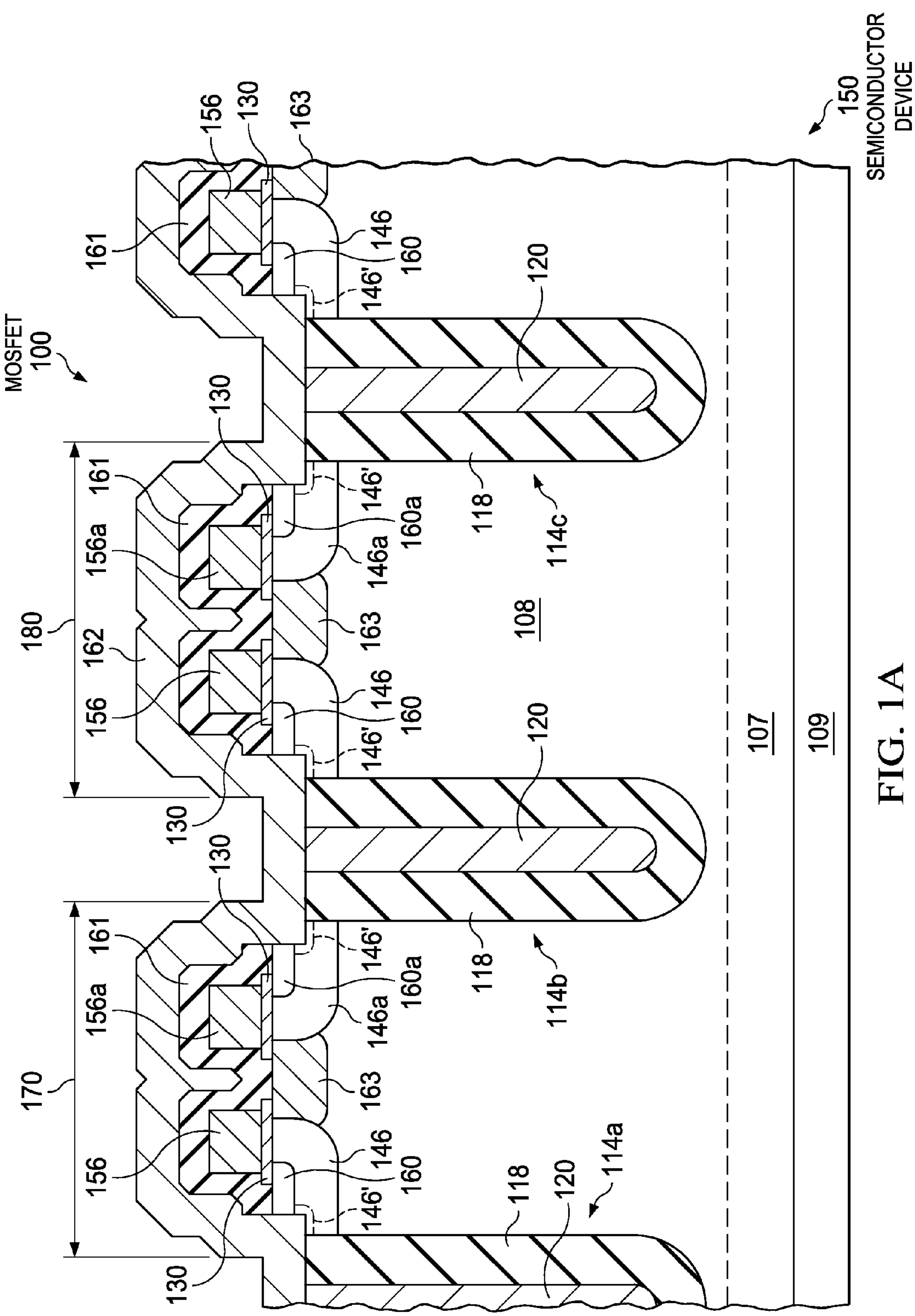
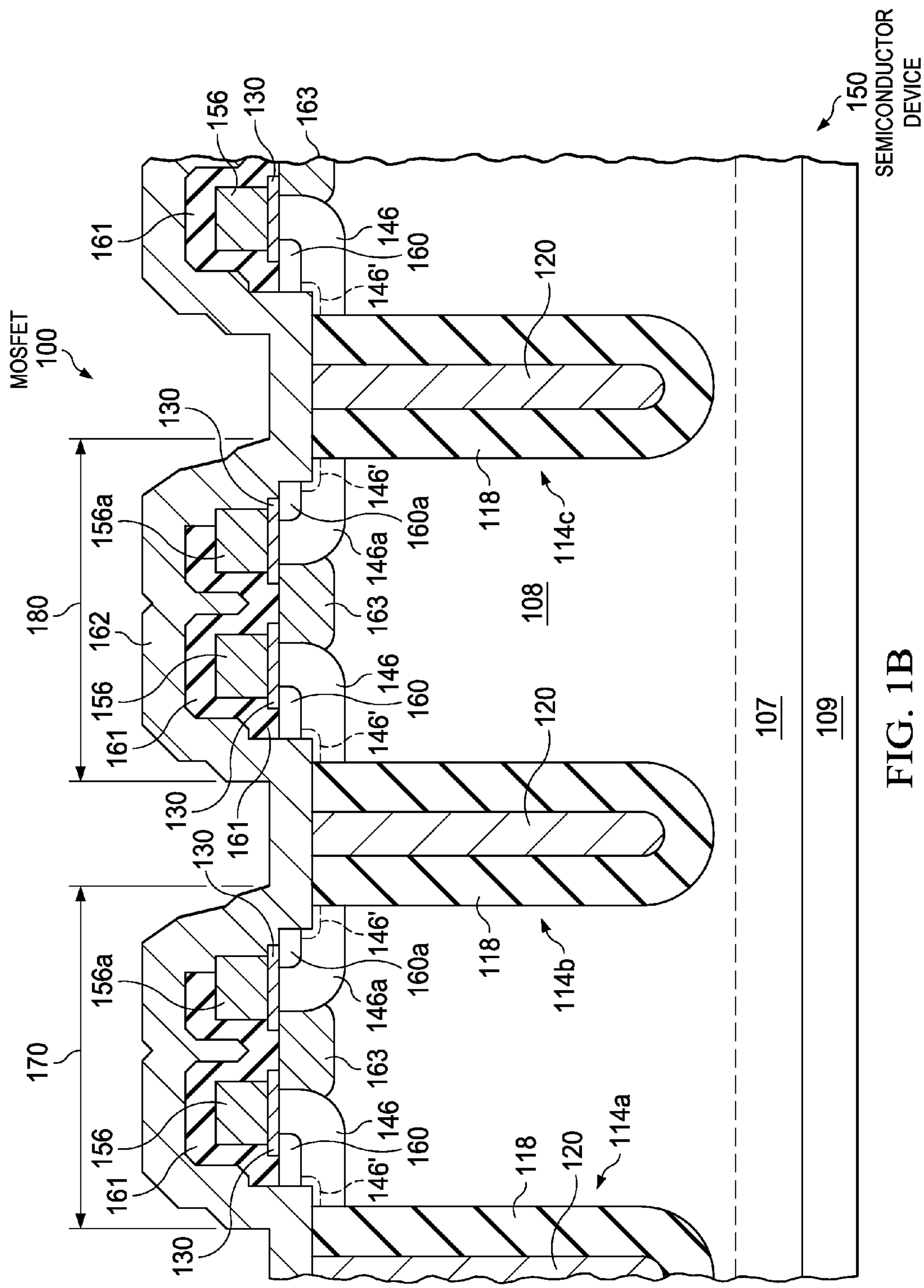

MOSFET
100
150
SEMICONDUCTOR
DEVICE
156
130
163
161
146
160
146'
120
118
114c
160a
146a
156a
180
162
108
107
109
170
114b
114a

FIG. 1A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146'
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114c
156a
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160a
180
162
108
107
109
170
114b
114a

FIG. 1B

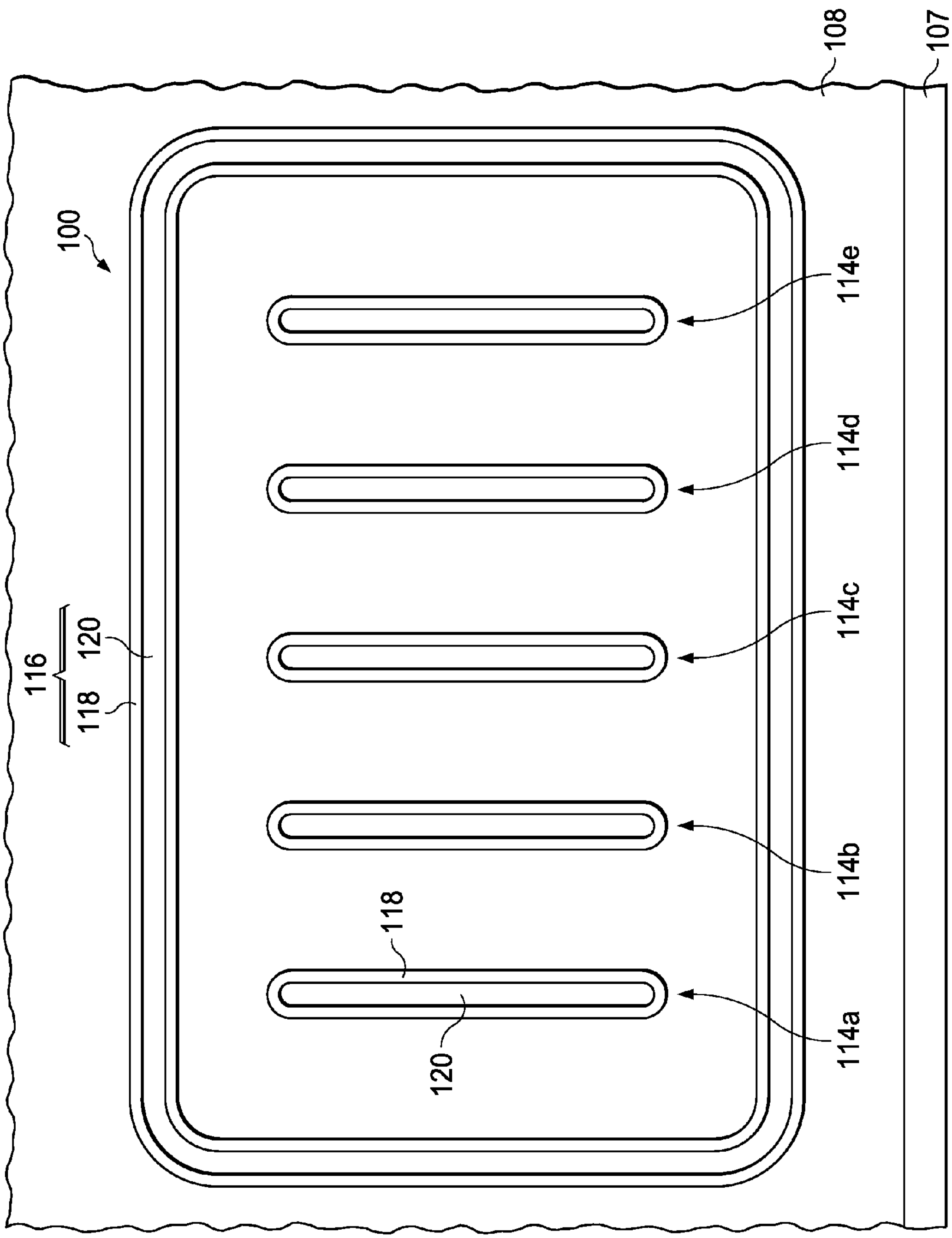
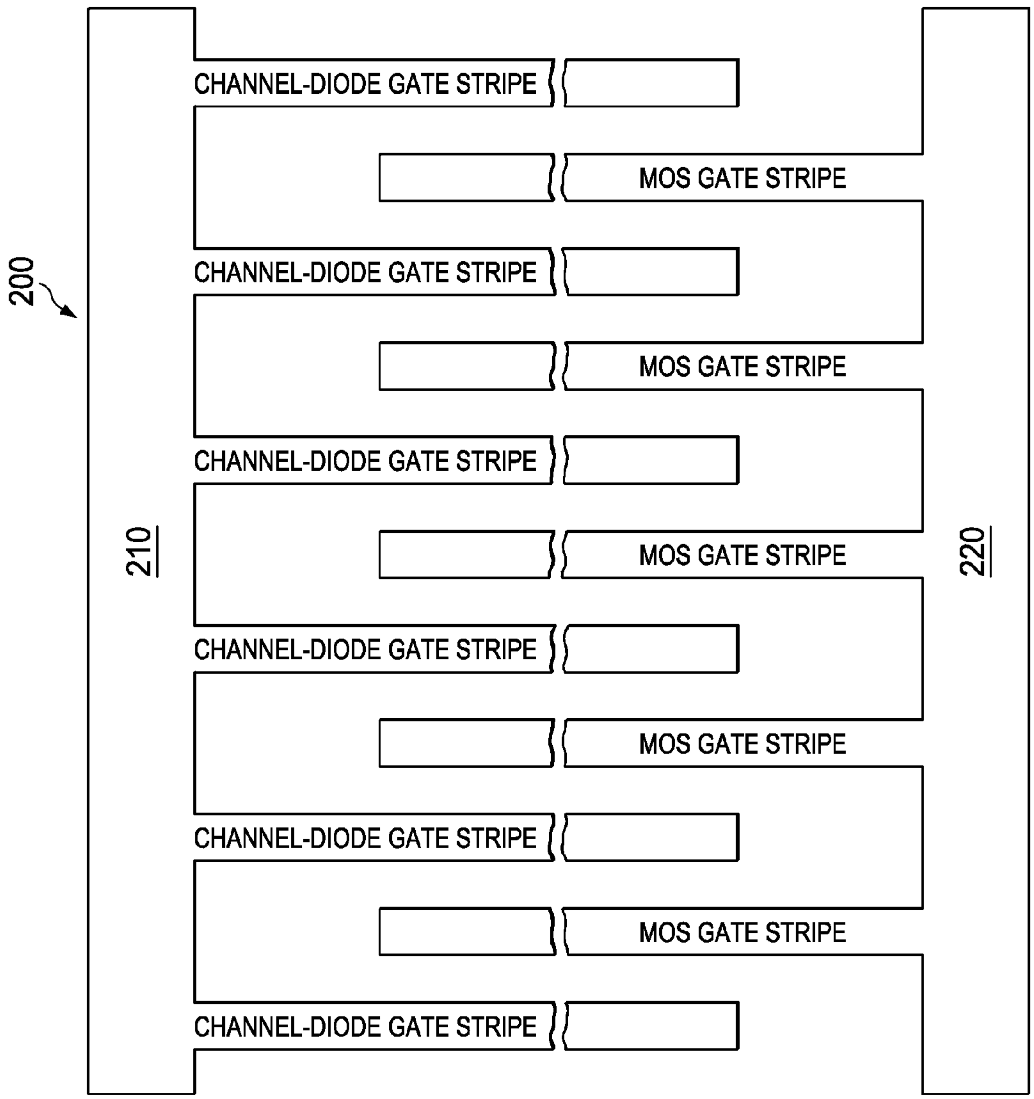


FIG. 1C


200
210
220
CHANNEL-DIODE GATE STRIPE
MOS GATE STRIPE
CHANNEL-DIODE GATE STRIPE
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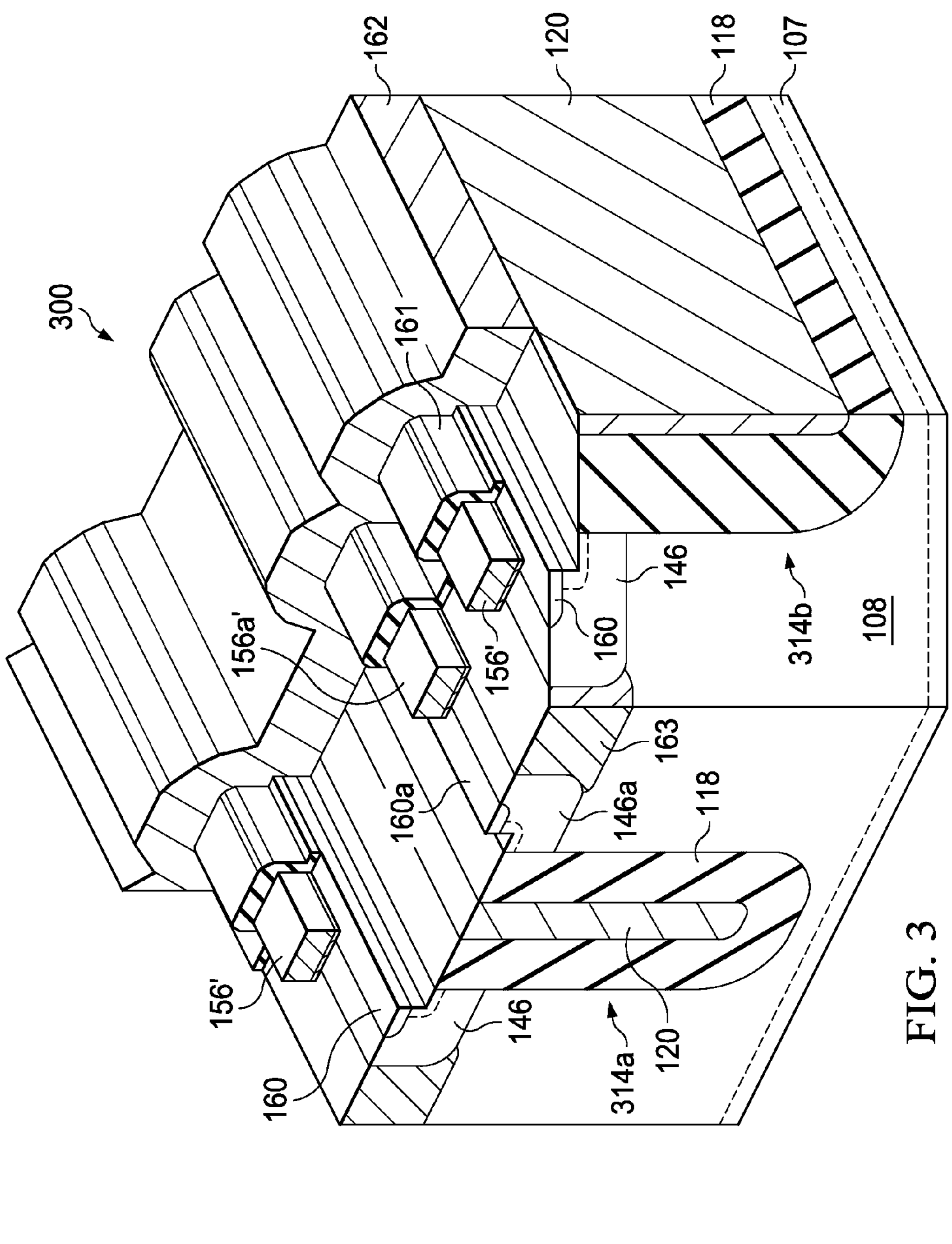
MOS GATE STRIPE
CHANNEL-DIODE GATE STRIPE
MOS GATE STRIPE
CHANNEL-DIODE GATE STRIPE
MOS GATE STRIPE
CHANNEL-DIODE GATE STRIPE

FIG. 2


300
162
120
118
107
161
146
314b
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160
156'
156a'
163
146a
118
160a
156'
146
120
314a
160

FIG. 3

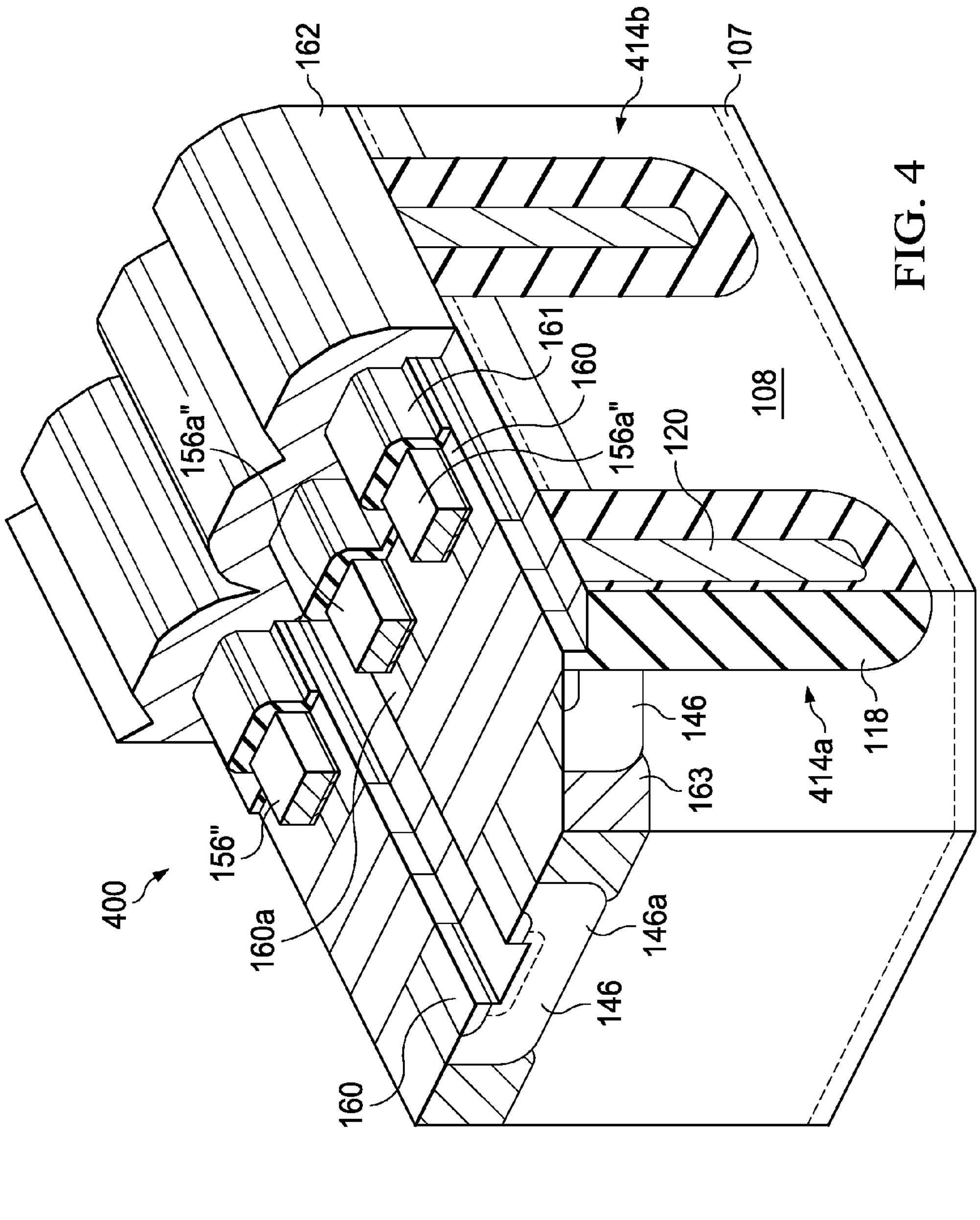
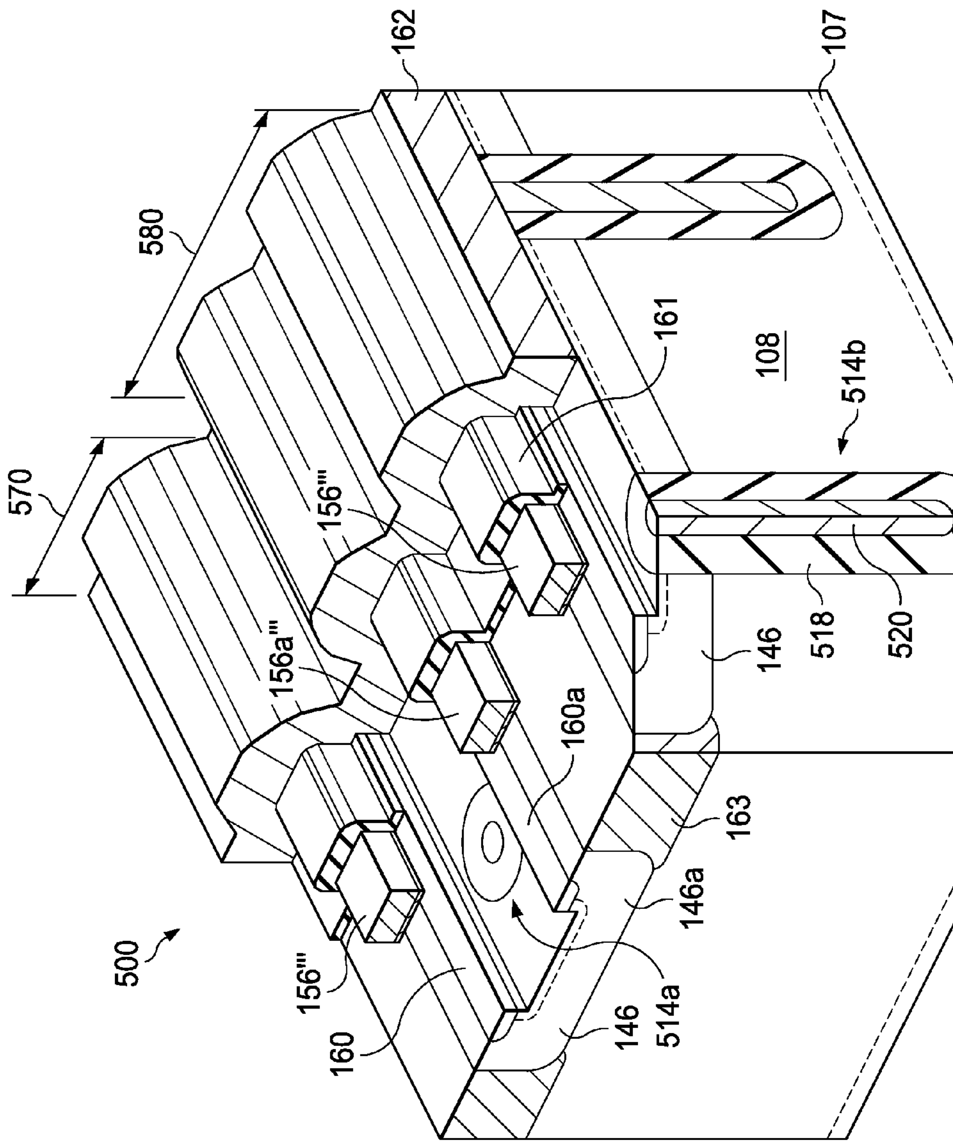

400
156"
160a
160
146
146a
163
146
414a
118
120
156a"
160
161
108
156a"
162
414b
107

FIG. 4


162
107
580
570
161
108
514b
156'''
156a'''
160a
146
518
520
163
146a
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160
146
514a

FIG. 5

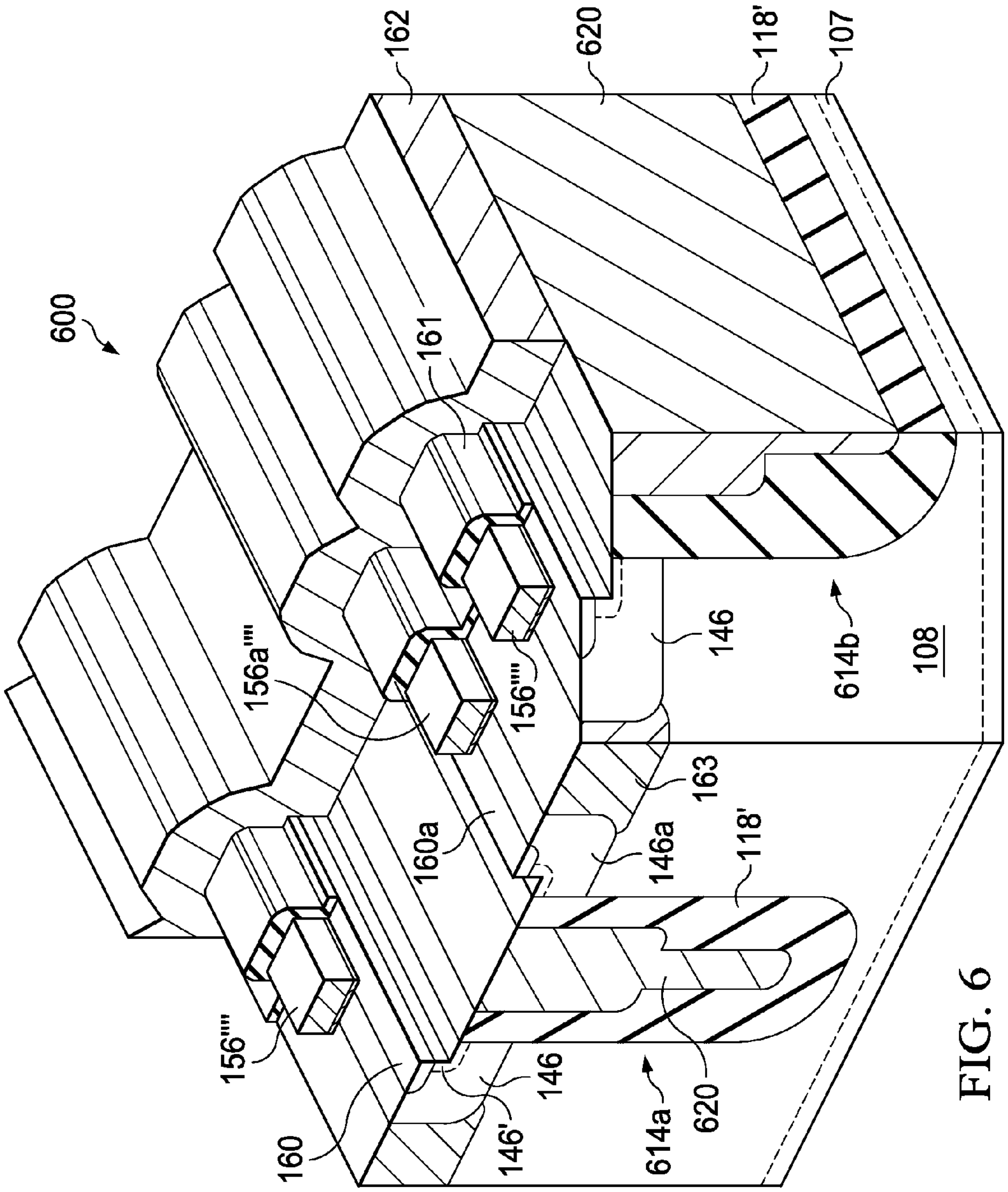
600
162
620
118'
107
161
156a''''
156''''
146
614b
108
163
160a
146a
118'
156''''
160
146'
146
614a
620

FIG. 6

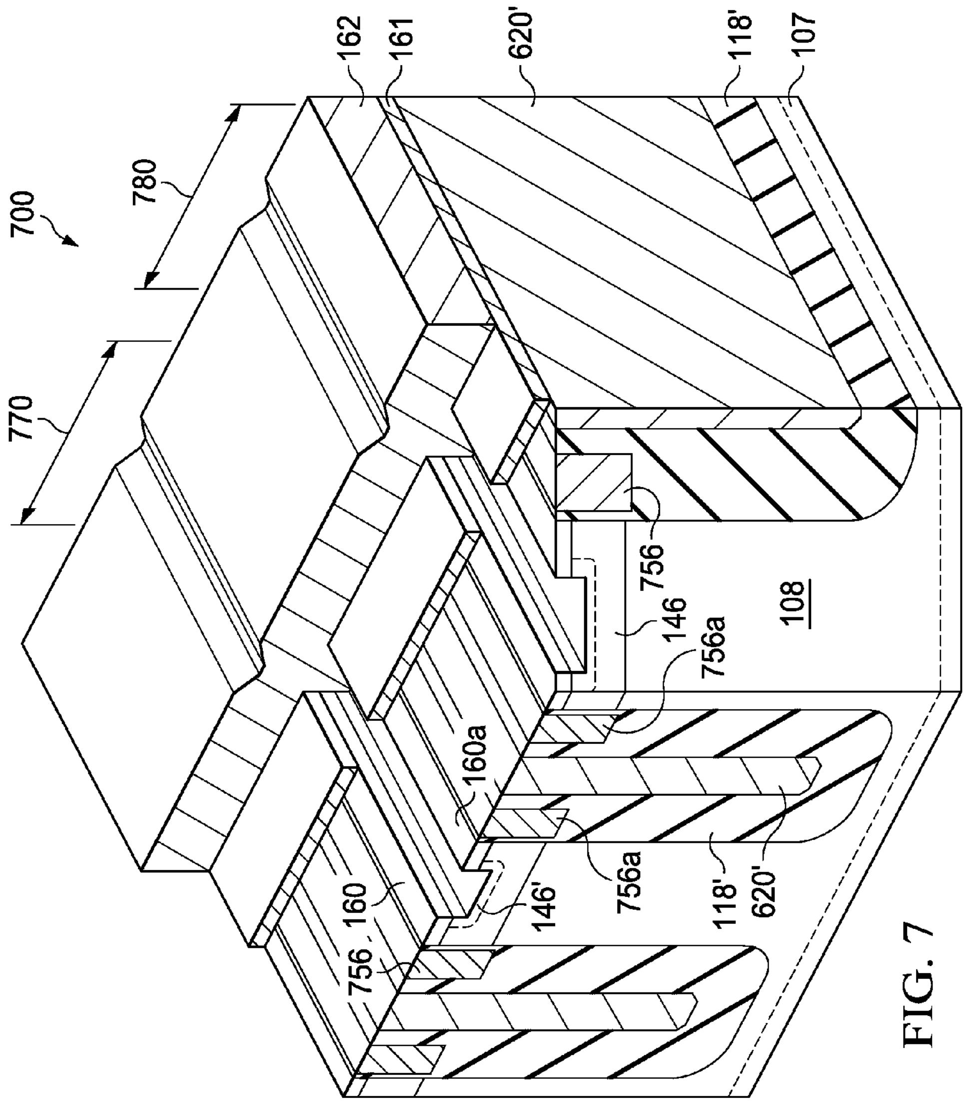
700
770
780
162
161
620'
118'
107
756
146
108
756a
160a
756a
118'
620'
160
146'
756
160

FIG. 7

MOSFET HAVING DUAL-GATE CELLS WITH AN INTEGRATED CHANNEL DIODE

FIELD

Disclosed embodiments relate to metal-oxide-semiconductor field-effect transistors (MOSFETs) having electrically conductive filler material (e.g., polysilicon) filled trenches as field plates.

BACKGROUND

Some power MOSFETS designs include dielectric lined polysilicon filled trenches as their gates. In this power MOSFET structure, the gate is buried in a trench etched in the semiconductor, such as a substrate comprising silicon. This arrangement results in a vertical channel.

Other power MOSFETS designs use dielectric lined polysilicon filled trenches as field plates and provide a substantially planar FET structure, where the trench polysilicon is connected to the source (and generally also the body). For example, these MOSFETs have a gate structure and a vertical drain drift region between polysilicon filled trenches configured to act as field plates sometimes referred to as "RESURF trenches". For purposes of this patent application, the term "RESURF" is understood to refer to a material which reduces an electric field in an adjacent semiconductor region. A RESURF region may be for example a semiconductor region with an opposite conductivity type from the adjacent semiconductor region. RESURF structures are described in Appels, et. al., "Thin Layer High Voltage Devices" Philips J, Res. 35 1-13, 1980.

The RESURF trenches contain a dielectric liner and are generally filled with doped polysilicon. In the active region for n-MOSFET, the RESURF trenches (hereafter "active area trenches") are polysilicon field plates which are electrically coupled to the source electrode. In the case of an n-MOSFET, there is a p-body region within an n-drift region on a substrate, where n-type dopants are in the source regions formed in the p-body region. The drain for the n-MOSFET can be a vertical drain drift region that uses the entire n-drift region below the p-body region that has a drain contact on the bottom of the substrate, which can be an n+ substrate.

Related U.S. application Ser. No. 13/744,097 to Kocon et al. hereafter "the '097 application" where Kocon is one of the inventors of this application as well, discloses the MOS device described above having a substantially planar gate structure on a drift region of a first conductivity type and a body region of a second conductivity type formed in the drift region, having sources for n-MOSFETs formed in the body region. A vertical drain drift region is positioned between active area trenches.

A contact metal stack makes electrical contact with a source region for the MOSFET at lateral sides of the contact structure, makes electrical contact with a body contact region at a bottom surface of contact structure, and makes electrical contact to the polysilicon field plates in the active area trenches. Another RESURF trench which is referred to as a "termination trench" is at a perimeter around the active area trenches.

SUMMARY

This Summary is provided to introduce a brief selection of disclosed concepts in a simplified form that are further described below in the Detailed Description including the drawings provided. This Summary is not intended to limit the claimed subject matter's scope.

Disclosed embodiments recognize a large percentage of power metal-oxide-semiconductor field-effect transistor (MOSFET) losses in power converter circuits are due to the switching loss caused by the presence of the inherent body diode (a PN junction) between the source and drain terminals, where the body region is shorted to the source. Such losses are present for both trench gate and planar gate MOSFET designs. The body diode is also recognized to induce circuit electromagnetic interference (EMI) and voltage spikes during operation that can be destructive to the MOSFET and the other power convertor circuit elements on the semiconductor device.

Disclosed embodiments relate to semiconductor devices including power MOSFETs including a plurality of MOSFET elemental cells (MOSFET cells) each having a planar (or lateral) split gate structure between active area trenches (RESURF trenches that function as field plates) including a first gate and a second gate, or a split trench gate, and a largely vertical drain drift region under the body region. One MOS gate is conventionally connected having separate contacts so that the gate, source and drain are electrically separated from its gate electrode which is referred to herein as a "MOS gate", while the other MOS gate has its gate electrode and source intentionally shorted (e.g., by metal or polysilicon) together with the body to provide a diode connected transistor referred to herein as an "integrated channel diode" having a gate electrode referred to as a "diode gate".

Although disclosed MOSFET cells are described as having a single MOS gate and a single diode gate, disclosed MOSFET cells can include more than one MOS gate and/or more than one diode gate. A disclosed integrated channel diode (which can also be termed a "pseudo-Schottky diode") functions as a rectifier diode in which when forward biased the forward current flows primarily through a thin layer or channel along the semiconductor surface of the device, rather than in the vertical direction through the bulk of the substrate.

As known in the art, a power MOSFET generally includes at least several hundred MOSFET cells electrically in parallel, typically several thousand MOSFET cells. Disclosed integrated channel diodes being MOSFET cells with its diode gates shorted to its source and body, blocks the flow of current which would otherwise drive its mobile carriers from the source to drain for, and allows current to freely flow in the direction for which carriers move (vertically).

A conventional silicon PN junction diode at room temperature has an offset (or turn-on) voltage of about 0.6 volts to 0.8 volts around room temperature before significant current begins to flow, because this is the voltage needed to overcome the built-in potential barrier of the junction. A disclosed integrated channel diode has a lower offset (or turn-on) voltage as compared to a conventional PN junction diode because the applied forward voltage being also applied to the diode gate acts as a gate bias which enhances the electrical conductivity of the channel region in the semiconductor surface under the diode gate, allowing carriers to flow through the channel without having to receive enough energy to "go over" the full height of the potential barrier. The lower offset voltage provided is advantageous because it results in less power loss, and more efficient operation for MOSFETs having disclosed integrated channel diodes as compared to conventional PN junction body diodes. Moreover, disclosed MOSFETs for power converter circuits reduce reverse recovery switching losses combined with lower EMI and peak voltage ringing compared to otherwise equivalent MOSFETs.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference will now be made to the accompanying drawings, which are not necessarily drawn to scale, wherein:

FIG. **1**A is a cross sectional view of a semiconductor device including a portion of a disclosed MOSFET having split gate planar cells showing two n-channel MOSFET cells, according to an example embodiment.

FIG. **1**B is a cross sectional view of the semiconductor device shown in FIG. **1**A along a cut where the diode gates of the cells contact the source metal along lengths of diode gate stripes, according to an example embodiment.

FIG. **1**C is a top view of an example disclosed MOSFET showing a termination trench surrounding a plurality of active area trenches.

FIG. **2** is a top view depiction showing an example MOSFET having split gate planar cells including alternating (interdigitated) diode gate and MOS gate contacts for a split gate embodiment having including integrated channel diode stripes and MOS gate stripes, according to an example embodiment.

FIG. **3** is a perspective cross sectional view of an example MOSFET having split gate planar cells including active area trenches which are oriented in the same direction as the diode gate stripes and MOS gate stripes, according to an example embodiment.

FIG. **4** is a perspective cross sectional view of an example MOSFET having split gate planar cells including active area trenches which are oriented 90° to a direction of the diode gate stripes and MOS gate stripes according to an example embodiment.

FIG. **5** is a perspective cross sectional view of an example MOSFET split gate planar cells including active area trench wells structures instead of active area trenches configured as stripes as disclosed above, according to an example embodiment.

FIG. **6** is a perspective cross sectional view of an example MOSFET split gate planar cells including alternating MOS gate stripes and diode gate stripes, with contacts at the ends of the respective gate stripes, according to an example embodiment.

FIG. **7** is a perspective cross sectional view of an example MOSFET having split trench gate cells including alternating MOS gate stripes and diode gate stripes having a shield framed by a trench dielectric liner between the cells, according to an example embodiment.

DETAILED DESCRIPTION

Example embodiments are described with reference to the drawings, wherein like reference numerals are used to designate similar or equivalent elements. Illustrated ordering of acts or events should not be considered as limiting, as some acts or events may occur in different order and/or concurrently with other acts or events. Furthermore, some illustrated acts or events may not be required to implement a methodology in accordance with this disclosure.

Also, the terms "coupled to" or "couples with" (and the like) as used herein without further qualification are intended to describe either an indirect or direct electrical connection. Thus, if a first device "couples" to a second device, that connection can be through a direct electrical connection where there are only parasitics in the pathway, or through an indirect electrical connection via intervening items including other devices and connections. For indirect coupling, the intervening item generally does not modify the information of a signal but may adjust its current level, voltage level, and/or power level.

FIG. **1**A is a cross sectional view of an example semiconductor device **150** built on an n-semiconductor surface (n-drift region) **108** of a substrate **107** including a portion of an n-channel MOSFET **100** (MOSFET **100**) showing two n-channel MOSFET split gate planar cells **170** and **180** with alternating MOS gate electrode stripes (shown in FIG. **1**A and hereafter referred to as "MOS gates" **156**) and diode gate electrode stripes (shown in FIG. **1**A and hereafter referred to as "diode gates" **156***a*), according to an example embodiment. The MOS gates **156** are for one gate of the MOSFET cells having a conventional separate gate, source, and drain, with the source tied to the body, which operates as a 3-terminal MOSFET, and the other gate is a diode gate configured as an integrated channel diode cell having a gate, source and drain, with the gate, source and body shorted together to operate as 2-terminal integrated channel diode (see, e.g., FIG. **1**B described below showing source metal shorting to the diode gates to the source and body and FIG. **3** described below showing a bus shorting the source to the diode gate and to the body). Although the MOSFETs described herein including MOSFET **100** are described as being n-channel MOSFETs, disclosed embodiments also include p-channel MOSFETs which can be achieved as known in the art by changing the semiconductor type dopings from p to n-type and from n to p type, with appropriate change in the doping levels.

MOSFET **100** includes n+ doped source regions shown as **160***a* for the diode gates **156***a* and *n*+ doped source regions **160** for the MOS gates **156**. MOSFET **100** includes p-doped body regions **146** for MOS gates **156** and p-doped body regions **146***a* for the diode gates **156***a*. As described below, p-doped body regions **146** and p-doped body region **146***a* can be doped differently. The p-doped body regions **146** and **146***a* have a p+ contact **146'**. As described below, the top metal shown as "source metal" **162** in FIG. **1**A can be connected to the source regions **160***a* associated with the diode gates **156***a*, source regions **160** associated with the MOS gates **156**, the diode gates **156***a*, and to the p-doped body **146** and p-doped body **146***a*.

N channel MOSFET cells **180** is shown including a split gate structure between active trench **114***b* and active trench **114***c*, an n-channel MOSFET cells **170** is shown including a split gate structure between active area trench (active trench) **114***a* and active trench **114***b*, where the diode gates **156***a* when connected by source metal **162** (not shown in FIG. **1**A) becomes the anode region of the integrated channel diode. The n-semiconductor surface (n-drift region) **108** on the substrate **107** shown doped n+ is the common drain of the n-channel MOSFET cells **170** and **180**, which becomes the cathode region of the integrated channel diode.

Disclosed integrated channel diodes have a significant advantage recognized herein in that they provide a faster recovery during the transition from forward conduction to reverse blocking as compared to a conventional PN junction. This occurs because the channel current for disclosed integrated channel diodes have only one kind of carrier, while the current across a conventional PN junction includes both kinds of carriers, both holes and electrons. After a PN junction diode has carried a forward current, the voltage-supporting region contains a mixture of both kinds of carriers, and cannot support a reverse voltage until enough time has passed for these excess carriers to recombine or to be removed by reverse current flow. This additional current during reverse recovery of the conventional PN junction diode is considered as power loss and a reason for circuit EMI noise and voltage oscillation. On the other side, forward current in the integrated channel diode is carried by only a single type of carrier, so the voltage-supporting region contains no excess carriers, and is essentially immediately ready to begin supporting reverse voltage when operated at a forward voltage below the PN junction barrier voltage.

The substrate **107** and/or n-drift region **108** more generally can comprise silicon, silicon-germanium, or other semiconductor material including III-V or II-VI materials. In one particular arrangement the n-drift region **108** is epitaxially oriented relative to the substrate **107**, such as n-epitaxial layer on an n+ substrate for NMOS, or as p-epitaxial layer on a p+ substrate for PMOS embodiments. Another example is a silicon/germanium (SiGe) epitaxially grown on a silicon substrate.

Active trenches **114***a-c* are shown formed in the n-drift region **108** and lined by a trench dielectric liner **118**. Active trenches **114***a*-**114***c* also include an electrically conductive filler material **120** that generally comprises doped polysilicon, which function as RESURF trenches. A termination trench (not shown in FIG. **1**A) generally sandwiches at least two sides of the plurality of active trenches as shown in FIG. **1**C as **116** described below. High temperature tolerant electrically conductive filler materials other than polysilicon can also be used for the trenches, such as tungsten. In the case of doped polysilicon, the polysilicon is generally doped (e.g. n+ or p+), which can be doped in-situ with the polysilicon deposition, or deposited undoped and then ion implanted with one or more dopant ions. The active trenches **114***a-c* include a contact which allows the source metal **162**, for example 2 μm to 5 μm of sputtered aluminum, to contact the electrically conductive filler material **120** at the top of the active trench. The source metal **162** can be replaced by other electrically conductive layers such as a polysilicon layer. The active trenches **114***a-c* can be 0.5 μm to 2 μm wide in one embodiment.

The trench dielectric liner **118** is a dielectric material which can comprise silicon oxide, or another dielectric material such as silicon nitride or silicon oxynitride, or a metal comprising high-k dielectric (k>5) material such as HfO_2. Although shown as a single layer, the trench dielectric liner **118** can comprise a relatively thin thermal silicon oxide layer (e.g., 50 to 100 nm) followed by a relative thick deposited dielectric layer (e.g., 200 nm to 400 nm of deposited silicon oxide).

A dielectric layer shown as an interlayer dielectric (ILD) layer **161** is shown over the top of the MOS gates **156** and diode gates **156***a*. In one embodiment the ILD layer **161** comprises a tetra-ethoxy-silane (TEOS) derived silicon oxide layer.

A planar split gate including MOS gate **156** and diode gate **156***a* is shown between active trenches for the MOSFET's cells, including MOSFET cell **180** that is between active trenches **114***b* and **114***c*. A p-doped body region **146** and p-doped region **146***a* are formed in the n-drift region **108**, which as noted above can be epitaxial relative to the substrate **107**. N-type dopants are in the source regions **160** and **160***a* formed in the p-doped body regions **146** and **146***a*. Although not shown, the respective gates can each include gate sidewall spacers. The gate dielectric layer is shown as **130**. A patterned polysilicon layer can provide MOS gate **156** and diode gate **156***a* which are both over the gate dielectric layer **130**.

N-type lightly doped drain (LDD) regions are shown as **163**. The drain for MOSFET device **100** is a vertical drain drift region that uses the entire n-drift region **108** below the p-doped body region **146** (so that no reference number for the drain is shown in FIG. **1**A), which has a drain contact (e.g. drain metal) **109** on the bottom side of the substrate **107**, where substrate **107** can be an n+ substrate, such as an n+ silicon substrate. For p-channel MOSFET embodiments, substrate **107** can be a p+ substrate, such as a p+ silicon substrate.

The polysilicon layer when used for the MOS and diode gates **156**, **156***a* may include 100 to 200 nanometers of polysilicon and possibly a layer of metal silicide (not shown) on the polysilicon, such as 100 to 200 nanometers of tungsten silicide. Other materials for the MOS and diode gates **156** and **156***a* are within the scope of this Disclosure.

Disclosed integrated channel diodes can be manufactured using the same threshold voltage (V_T) as the MOSFET cell portion by each having the same p-doped body region **146** doping. In this arrangement typically no changes are needed to the process flow, since shorting of diode gate to the source contact (and body contact) can be performed through a single contact mask layout change. However, in another embodiment, the performance of the integrated channel diode can be further improved in performance if the V_T of the integrated channel diode is lowered in absolute value (lower for NMOS or made less negative for PMOS). The reason is that a lower threshold in absolute value results in the integrated channel diode having lower V_f (forward voltage drop) due to being turned on at lower forward bias voltage. Also, the integrated channel diode will conduct more current than the conventional MOSFET cell portion, due to being lower Vf. An additional benefit as described above is lower reverse recovery due to most of current being MOS-gated diode current rather than parasitic MOSFET's body diode.

V_T lowering for disclosed integrated channel diodes can be implemented by adjustment of body or source implant in the integrated channel diode area only. In one embodiment the p-doped body region **146** has a different doping level for the MOS transistor cell portion as compare to the integrated channel diode cell portion. For example, the p-body region for the MOS gate transistors for NMOS embodiments can be have a doping level of about 2 or 3×10^{17} cm^{-3}, as compared to a lower doping level by at least a factor of 2, such as around 5×10^{16} cm^{-3} for the diode gate transistor to provide a lower V_T. For PMOS embodiments the n-body region for the MOS gate transistors can have a doping level of about 1×10^{17} cm^{-3} to 2×10^{17} cm^{-3}, as compared to a lower doping level by at least a factor of 2, such as around 3×10^{16} cm^{-3} to 5×10^{16} cm^{-3} for the diode gate transistor to provide a lower $|V_T|$.

FIG. **1**B is a cross sectional view of the semiconductor device **150** shown in FIG. **1**A along a cut where the diode gates **156***a* of the cells of the MOSFET **100** contact the source metal **162** along lengths of diode gate stripes, according to an example embodiment. The ILD **161** can be seen to terminate on the top of the diode gates **156***a* to allow the source metal **162** to short to the diode gate **156***a* along the sidewall of the diode gate **156***a* to its source regions **160***a* and p-doped body region **146***a*.

FIG. **1**C is a top view of the MOSFET **100** in FIGS. **1**A and **1**B modified to show a termination trench **116** surrounding a plurality of active trenches shown as active trenches **114***a*, **114***b*, **114***c*, **114***d* and **114***e*. Termination trench **116** includes trench dielectric liner **118** and electrically conductive filler material **120** therein. As noted above, although not shown in FIG. **1**C, a planar split gate including a MOS gate **156** and a diode gate **156***a* is between adjacent active trenches for each of the MOSFET cells. The termination trench **116** can have the same width as the active trenches **114***a*, **114***b*, **114***c*, **114***d* and **114***e*. Although not shown, the termination trench **116** is generally electrically connected to at least one of the active trenches **114***a*, **114***b*, **114***c*, **114***d* and **114***e*, where the active trenches are electrically connected to a source region **160** or **160***a* (such as shown in FIG. **1**A and FIG. **1**B).

FIG. **2** is a top view depiction of an example MOSFET **200** (MOSFET **200**) having split gate planar cells including alternating (interdigitated) diode gate and MOS gate contacts including integrated channel diode stripes and MOS gate stripes, according to an example embodiment. In this embodiment, on one end of the MOSFET **200** a first bus **210** that can comprise polysilicon, or metal (aluminum, copper or tungsten) ties (shorts) together all the source electrodes (and the bodies) to all of the diode gate stripes of the integrated channel diodes, while on the opposite end a second bus **220** that can also comprise polysilicon or metal ties (shorts) together all the MOS gate stripes. Although as shown in FIG. **2** all polysilicon gate stripes for both the diode gate stripes and the MOS gate stripes are each connected by common bus, in an alternate design there can be individual contacts to each stripe. Although shown as MOS gate stripes alternating with diode gate stripes, there can also be a smaller or larger percentage of diode gates relative to MOS gates by adjustment of the gate contact ratio between the first bus **210** and the second bus **220**.

FIG. **3** is a perspective cross sectional view of an example n-channel MOSFET **300** (MOSFET **300**) having split gate planar cells including active trenches shown as **314***a* and **314***b* including a trench dielectric liner **118** (e.g., silicon oxide) and electrically conductive filler material **120** (e.g., polysilicon) which are oriented in the same direction as the diode gate stripes **156***a*' and MOS gate stripes **156**', according to an example embodiment. The diode gate stripe **156***a*' and other diode gate stripes can all be shorted on one end to the source regions **160**, **160***a* by the source metal **162** shown (which as noted above can also be shorted by other electrically conductive materials such as polysilicon). The MOS gate stripes **156**' of respective cells can be shorted together on either end by metal or polysilicon.

FIG. **4** is a perspective cross sectional view of an example MOSFET **400** (MOSFET **400**) having split gate planar cells including active trenches shown as **414***a* and **414***b* including a trench dielectric liner **118** (e.g., silicon oxide) and electrically conductive filler material **120** (e.g., polysilicon) which are oriented 90° relative to a direction of the diode gate stripes **156***a*" and MOS gate stripes **156**" according to an example embodiment. The diode gate stripe **156***a*" and other diode gate stripes can all be shorted to the source regions **160**, **160***a* and the p-doped body regions **146**, **146***a* by the source metal **162** shown.

FIG. **5** is a perspective cross sectional view of an example n-channel MOSFET **500** (MOSFET **500**) having split gate planar cells including active trench wells **514***a* and **514***b* embodied as discrete polysilicon filled dielectric lined "well" structures instead of active trenches configured as stripes as disclosed above, according to an example embodiment. Analogous to the active trenches disclosed above, trench wells **514***a* and **514***b* include a dielectric liner **518** (e.g., silicon oxide) and electrically conductive filler material **520** (e.g., polysilicon). A diode gate stripe is shown as **156***a*''' and MOS gate stripes as **156**'''. In this embodiment there are thus a plurality of active trench wells along the length between the diode gate stripe **156***a*''' of one MOSFET cell shown as **580** and the MOS gate stripe **156**''' of an adjacent MOSFET cell shown as **570**.

FIG. **6** is a perspective cross sectional view of an example MOSFET **600** (MOSFET **600**) having split gate planar cells including alternating MOS gate stripes **156**"" and a diode gate stripe **156***a*"", with gate contacts at the ends of the respective gate stripes, according to an example embodiment. MOSFET **600** also is shown including trenches **614***a* and **614***b* having a dual-width shield **620** configured with the electrically conductive filler material such as polysilicon providing a wider thicker surface portion and a reduced width portion below the wider thicker surface portion. Shield **620** is shown framed by a trench dielectric liner **118**' (e.g., silicon oxide), with contacts to the shield **620** along the length of the trenches **614***a* and **614***b*.

FIG. **7** is a perspective cross sectional view of an example MOSFET **700** having split trench gate cells **770** and **780** including alternating MOS gate stripes **756** and diode gate stripes **756***a* having a shield **620**' framed by a trench dielectric liner **118**' (e.g., silicon oxide), between the cells, according to an example embodiment. In this MOSFET **700**, the MOS gate stripes **756** and diode gate stripes **756***a* are buried in a trench etched in the n-semiconductor surface (n-drift region) **108** of the substrate **107**. The source metal **162** shown provides contact to the diode gate stripes **756***a*, the p-body regions **146**, and the source regions **160** and **160***a*. There are also contacts to the MOS gate stripes **756** and contacts to the shields **620**' at their ends (not shown). The doping in p-body region **146** can be lower proximate to the diode gates as compared to proximate to the MOS gates as disclosed above for planar gate embodiments.

Numerous variations to disclosed embodiments beyond those disclosed above are possible. For example, the MOSFET **600** shown in FIG. **6** or MOSFET **700** shown in FIG. **7** can be modified to have localized contacts to the shields **620** or **620**' instead of along the length of the shield stripe.

Disclosed process flows to implement disclosed MOSFETs provide ease of implementation with the ability to change a single contact mask change to enable formation of disclosed integrated channel diodes for one of the gates in the dual gate cells. For the embodiment described above having a lower Vt integrated channel diodes as compared to the MOS gates, the process will generally add another step to allow |Vth| lowering, such as by adjustment of a p-body (for NMOS) doping (e.g., implantation) or n-body doping (e.g., implantation) for PMOS, or a source implant in the integrated channel diode area only.

Disclosed embodiments can be used to form semiconductor die that may be integrated into a variety of assembly flows to form a variety of different devices and related products. The semiconductor die may include various elements therein and/or layers thereon, including barrier layers, dielectric layers, device structures, active elements and passive elements including source regions, drain regions, bit lines, bases, emitters, collectors, conductive lines, conductive vias, etc. Moreover, the semiconductor die can be formed from a variety of processes including bipolar, Insulated Gate Bipolar Transistor (IGBT), CMOS, BiCMOS and MEMS. The semiconductor die can also be a discrete die.

Those skilled in the art to which this disclosure relates will appreciate that many other embodiments and variations of embodiments are possible within the scope of the claimed invention, and further additions, deletions, substitutions and modifications may be made to the described embodiments without departing from the scope of this disclosure.

The invention claimed is:

1. A semiconductor device, comprising:

a substrate;

a metal oxide semiconductor field effect transistor (MOSFET) cell including:

a drift region of a first conductivity type in the substrate;

active trenches formed adjacent to said drift region, said active trenches including an electrically conductive filler material surrounded by a trench dielectric liner;

a split gate comprising a MOS gate and a diode gate over said drift region and between said active trenches, said split gate using said active trenches as field plates;

a body region of a second conductivity type opposite from said first conductivity type abutting said active trenches, and the body region including a first body region proximate to said MOS gate and a second body region proximate to said diode gate;

a source region of said first conductivity type formed in said body region, the source region including a first source portion proximate to said MOS gate and a second source portion proximate to said diode gate;

a drain contact formed on a bottom side of said substrate opposing from the split gate, and

a connector connecting said diode gate to said second source portion to form a channel diode integrated to a MOSFET controlled by said MOS gate, wherein said MOS gate is electrically isolated from said first source portion.

2. The semiconductor device of claim **1**, wherein said second body region is lighter in doping by at least a factor of two (2) as compared to said first body region.

3. The semiconductor device of claim **1**, further comprising a termination trench abutting at least two vertical sides of said MOSFET cell.

4. The semiconductor device of claim **1**, wherein said connector comprises a metal.

5. The semiconductor device of claim **1**, wherein said connector comprises doped polysilicon.

6. The semiconductor device of claim **1**, wherein said substrate comprises silicon.

7. The semiconductor device of claim **1**, further comprising a first bus connecting said MOS gate of said MOSFET cell and a second bus connecting said diode gate of said MOSFET cell and to said second source portion.

8. The semiconductor device of claim **1**, wherein said MOS gate is configured as a MOS gate stripe and said diode gate is configured as a diode gate stripe, wherein said active trenches are aligned in parallel with said MOS gate stripe and said diode gate stripe.

9. The semiconductor device of claim **1**, wherein said MOS gate is configured as a MOS gate stripe and said diode gate is configured as a diode gate stripe, wherein said active trenches are aligned perpendicular to said MOS gate stripe and said diode gate stripe.

10. The semiconductor device of claim **1**, wherein said active trenches comprise active trench wells.

11. The semiconductor device of claim **1**, wherein said active trenches each includes an upper portion adjacent to a top surface of the substrate and a lower portion below the upper portion such that the upper portion is wider than the lower portion.

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